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James J. Stipanuk
Semiconductor Components Industries L.L.C.
Patent Administration Dept - MD/A700
P.O. Box 62890
Phoenix, AZ 85082-2890

EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,392	HADIZAD, PEYMAN	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 6th, 2005 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-6, 8-13, and 15-20) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-13, and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blanchard et al. (U.S. Patent 6,750,104) in view of Blanchard (U.S Patent 4,914,058).

In re claim 1, **Blanchard et al.** '104 disclose a method of making a semiconductor vertical FET device comprising the steps of:

providing a body of semiconductor material **501** comprising a first conductivity type (n-type), wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain

contact **D**; forming a first trench **520** in the body of semiconductor material **501** and extending from the upper surface, wherein the first trench **520** has a first width (**unlabeled**), a first depth (**unlabeled**) from the upper surface, first sidewalls (**unlabeled**), and a first bottom surface (col. 4, lines 30-40 and FIG. 4A);

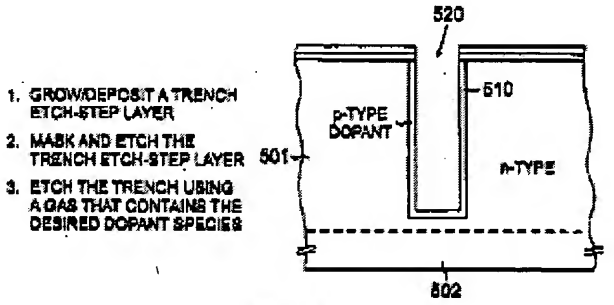


FIG. 4A

forming a first source region **7** in the body of semiconductor material **501** extending from the upper surface and spaced apart from the first trench **520** by a portion of the body of semiconductor material; introducing a dopant (Boron) of a second conductivity type (p-type) into at least a portion of the second sidewalls and the second bottom surface to form a doped gate region **512** wherein the doped gate region extends into the body of the semiconductor material (col. 4, lines 50-65 and FIG. 4B);

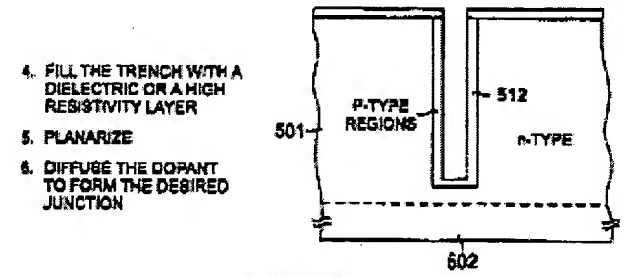
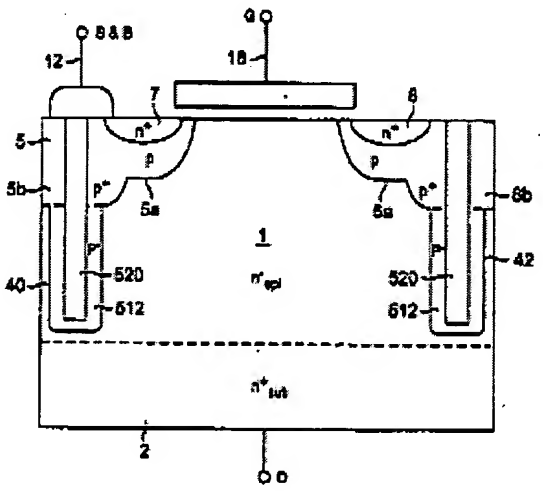


FIG. 4B

forming a first passivation layer over the doped gate region (col. 4, lines 50-57); and forming a second passivation layer over the first passivation layer thereby filling at least the trench (col. 4, lines 58-65 and FIG. 5).



THE DOPANT DISTRIBUTION OF A HIGH VOLTAGE VERTICAL DMOS TRANSISTOR WITH A RELATIVELY LOW ON-RESISTANCE

FIG. 5

Blanchard et al. '104 does not explicitly disclose forming a second trench within the first trench, wherein the second trench has a second width, a second depth from the first surface, second sidewalls and a second bottom surface.

Blanchard '058, however, discloses a method of making a semiconductor vertical FET device comprising the steps of: providing a body of semiconductor material comprising a first conductivity type (n-type), wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact; forming a first trench **31** in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width

(unlabeled), a first depth (unlabeled) from the upper surface, first sidewalls **41**, and a first bottom surface **42** (col. 3, line 60 to col. 5, line 3 and FIGS. 4a-b);

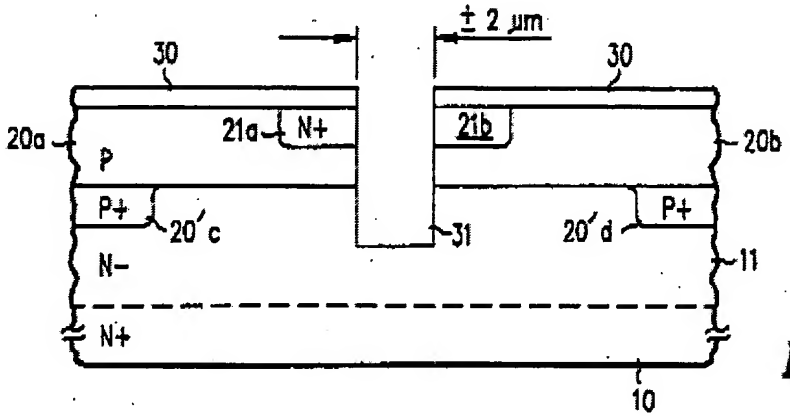


FIG. 4b

forming a second trench (unlabeled) within the first trench, wherein the second trench has a second width (unlabeled), a second depth (unlabeled) from the first surface, second sidewalls **43** and a second bottom surface **42a** (col. 5, lines 4-32 and FIG. 4g);

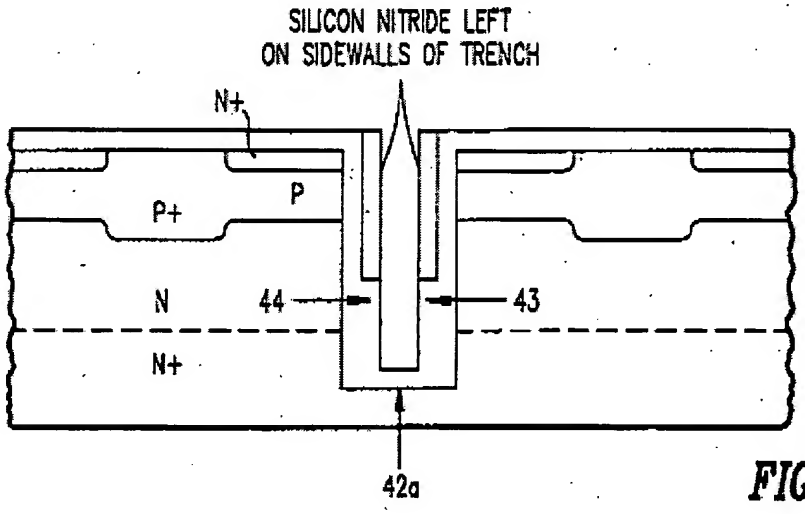


FIG. 4g

forming a first source region **21a** in the body of semiconductor material extending from the upper surface and spaced apart from the first trench (col. 5, line 33 to col. 6, line 37 and FIGS 3-10).

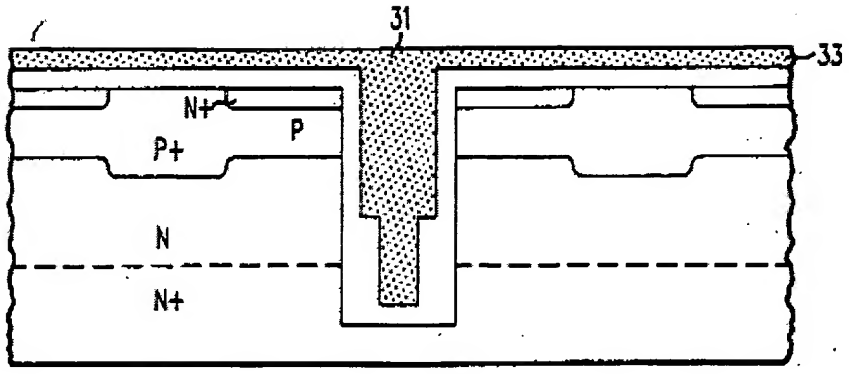


FIG. 4h

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Blanchard et al. '104 and Blanchard '058 to enable the process of forming a second trench within the first trench of Blanchard et al. '104 to be performed and furthermore to obtain a device which has a vertical gate and a planar surface (col. 2, lines 16-20, Blanchard '058).

In re claim 2, **Blanchard et al.** '104 discloses that the step of providing the body of semiconductor material comprises providing a III-V semiconductor substrate having a first dopant concentration and a first epitaxial layer formed on a surface of the semiconductor substrate, wherein the first epitaxial layer has a second dopant concentration less than the first dopant concentration (col. 4, lines 30-40 and FIG. 4A).

In re claim 3, **Tews et al.** (U.S. Patent 6,335,247) provide evidence that the step of providing the body of semiconductor material comprises providing a body of semiconductor material comprising GaAs (gallium arsenide) is well-known to one of ordinary skill in the art at the time of the invention was made (col. 5, lines 12-33 and FIG. 3A).

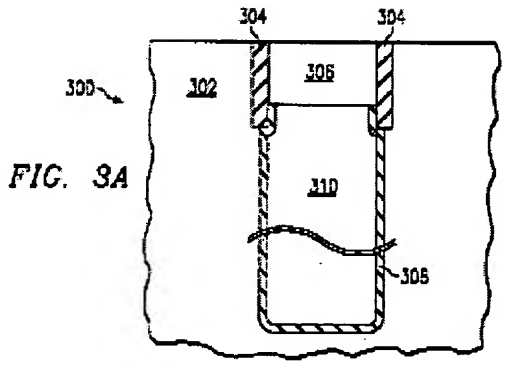


FIG. 3A

In re claim 4, **Blanchard** '058 discloses that the step of forming the second trench comprises the steps of: depositing a spacer layer **40** over the upper surface and the first trench **31**; etching back the spacer layer to form spacers that cover first sidewalls **41** and a portion of the first bottom surface **42** leaving a self-aligned opening in the dielectric layer to expose a remaining portion of the bottom surface; and etching the second trench through the opening (col. 5, lines 4-10 and FIG. 4f).

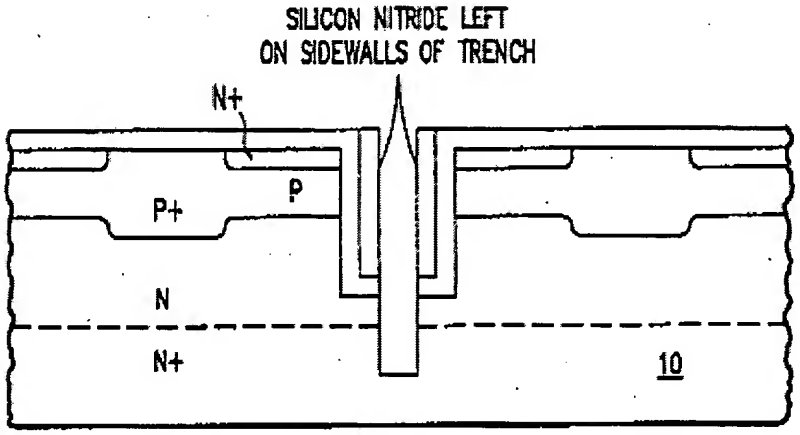


FIG. 4f

In re claim 5, **Blanchard et al.** '104 discloses that the step of introducing the dopant of the second conductivity type comprises implanting the dopant into the second sidewalls and the second bottom surface (col. 4, lines 50-65 and FIG. 4B).

In re claim 6, **Plumton et al.** (U.S. Patent 6,229,197) provide evidence that the step of implanting the dopant species includes implanting one of beryllium and carbon is well-known to one of ordinary skill in the art at the time of the invention was made (col. 7, lines 16-44).

In re claim 8, **Blanchard et al.** '104 disclose that the step of forming the second passivation comprises the steps of: depositing a dielectric material over the first passivation layer; and planarizing the dielectric material to form the second passivation layer (col. 4, lines 58-65).

In re claim 9, **Blanchard et al.** '104 disclose that the method of claim 1 further comprising the step forming a second source region **8** in the body of semiconductor material spaced apart from the first trench **520** by another portion of the body of semiconductor material, wherein the first trench **520** is between the first **7** and the second sources **8** (FIG. 5).

In re claim 10, **Blanchard et al.** '104 disclose that the step of forming the first trench **520** includes etching the first trench using one of reactive ion etching (RIE) and electron cyclotron resonance etching (col. 4, lines 30-50 and FIG. 4A).

In re claim 11, **Blanchard** '058 disclose that the step of forming the second trench includes etching the second trench using one of reactive ion etching and electron cyclotron resonance etching (col. 5, lines 3-36).

In re claim 12, **Blanchard et al.** '104 disclose a process of making a compound semiconductor vertical junction FET device comprising the steps of: forming a first groove **520** in a compound semiconductor layer of a first conductivity type (n-type),

wherein the first groove has first sidewalls, and a first lower surface, and wherein the first groove extends from a first surface of the compound semiconductor layer (col. 4, lines 30-40 and FIG. 4A);

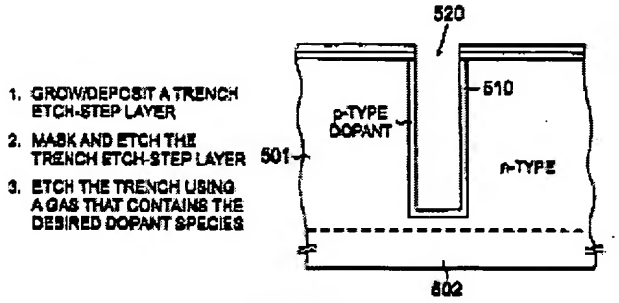


FIG. 4A

doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant (p-type) to form a doped gate region **512** in the compound semiconductor layer; forming a first source region **7** of the first conductivity type (n-type) in the compound semiconductor layer adjacent to the first groove **520** (col. 4, lines 50-65 and FIG. 4B);

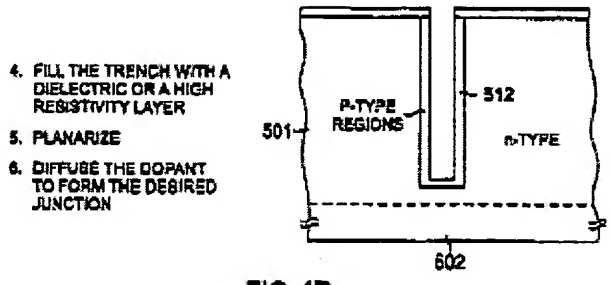
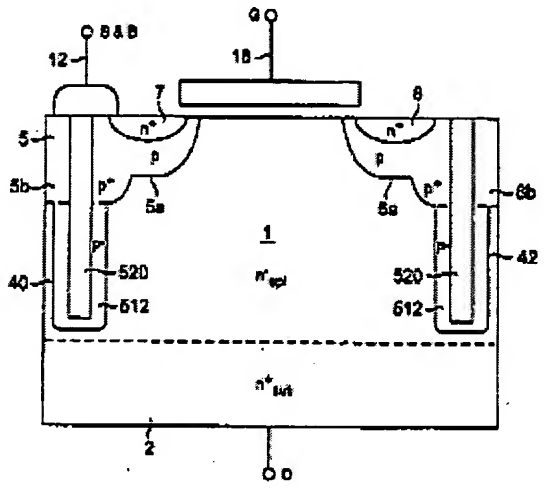


FIG. 4B

forming a source contact **12** to the first source region **7**; filling the second groove and at least a portio of the first groove with a passivation layer (col. 4, lines 58-65 and

FIG. 5); forming a gate contact **18** coupled to the doped gate region **512**; and forming a drain contact **D** on a second surface of the compound semiconductor layer (col. 5, lines 23-54 and FIG. 5);



THE DOPANT DISTRIBUTION OF A HIGH VOLTAGE VERTICAL DMOS TRANSISTOR WITH A RELATIVELY LOW ON-RESISTANCE

FIG. 5

Blanchard et al. '104 does not explicitly disclose forming a second groove within the first groove, wherein the second groove has second sidewalls and a second lower surface.

Blanchard '058, however, discloses a method of making a semiconductor vertical FET device comprising the steps of: providing a body of semiconductor material comprising a first conductivity type (n-type), wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact; forming a first trench **31** in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width

(unlabeled), a first depth (unlabeled) from the upper surface, first sidewalls **41**, and a first bottom surface **42** (col. 3, line 60 to col. 5, line 3 and FIGS. 4a-b);

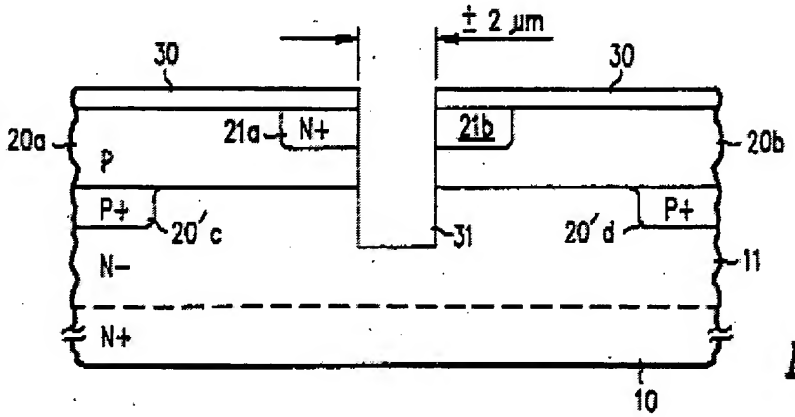


FIG. 4b

forming a second trench (unlabeled) within the first trench, wherein the second trench has a second width (unlabeled), a second depth (unlabeled) from the first surface, second sidewalls **43** and a second bottom surface **42a** (col. 5, lines 4-32 and FIG. 4g);

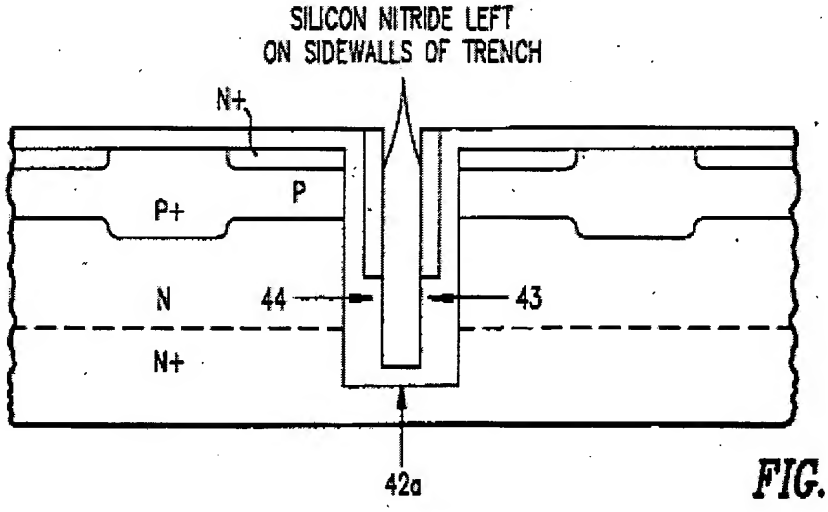


FIG. 4g

forming a first source region **21a** in the body of semiconductor material extending from the upper surface and spaced apart from the first trench (col. 5, line 33 to col. 6, line 37 and FIGS 3-10).

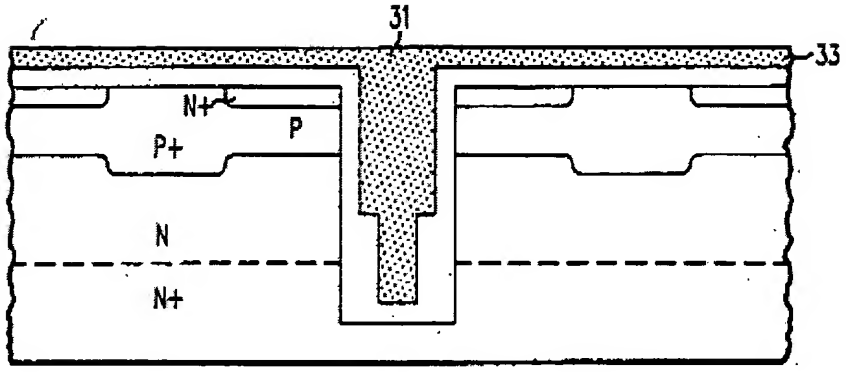


FIG. 4h

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Blanchard et al. '104 and Blanchard '058 to enable the process of forming a second groove within the first groove of Blanchard et al. '104 to be performed and furthermore to obtain a device which has a vertical gate and a planar surface (col. 2, lines 16-20, Blanchard '058).

In re claim 13, **Tews et al.** (U.S. Patent 6,335,247) provide evidence that the step of forming the first groove includes forming the first groove in a compound semiconductor layer comprising one of GaAs (gallium arsenide) and InP is well-known to one of ordinary skill in the art at the time of the invention was made (col. 5, lines 12-33 and FIG. 3A).

In re claim 15, **Blanchard et al.** '104 disclose that the step of doping the second lower surface and at least a portion of the second sidewalls includes ion implanting a second conductivity type dopant species Boron (p-type) (col. 4, lines 40-65).

In re claim 16, **Blanchard** '058 discloses that the step of forming the second groove comprises the steps of: forming spacers on the first sidewalls **41** leaving an

opening over the first lower surface **42**; and etching the second groove in the compound semiconductor through the opening (col. 5, lines 4-24 and FIGS. 4d-f).

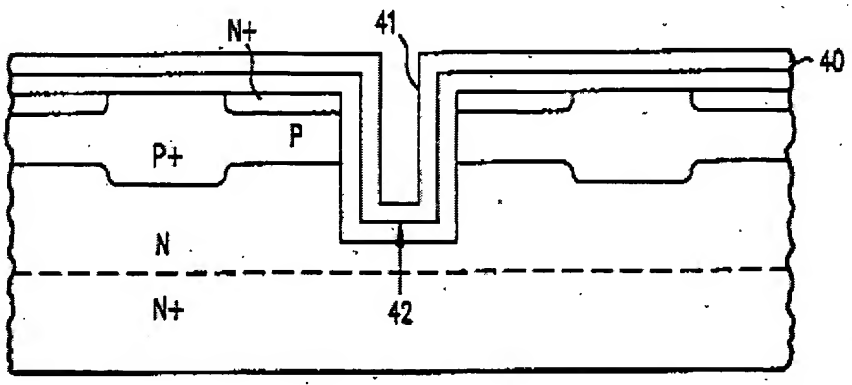


FIG. 4d

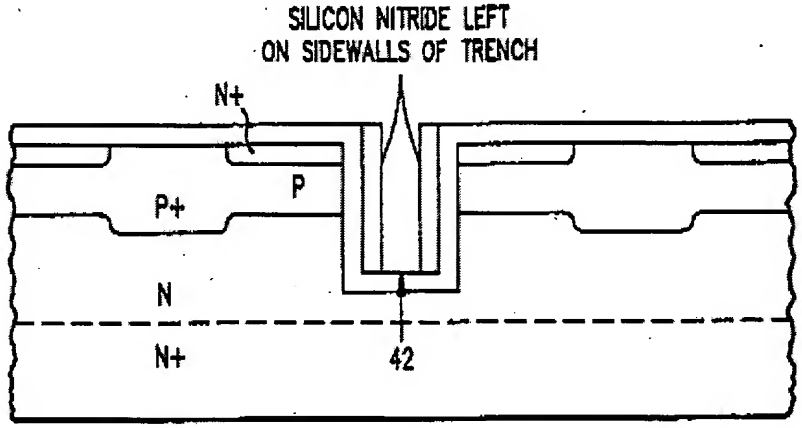


FIG. 4e

In re claim 17, **Blanchard** '058 discloses that the steps of forming the first and second grooves including forming first and second grooves having substantially straight sidewall surfaces (FIG. 4f).

In re claim 18, **Blanchard et al.** '104 disclose a method for forming a compound semiconductor FET device comprising the steps of: providing a body of compound semiconductor material including a support wafer **502** of a first conductivity type (n-type) and a first dopant level and an epitaxial layer **501** formed over the support wafer **502**,

wherein the epitaxial layer is of the first conductivity type (n-type) and has a second dopant level lower than the first dopant level (col. 4, lines 30-40 and FIG. 4A);

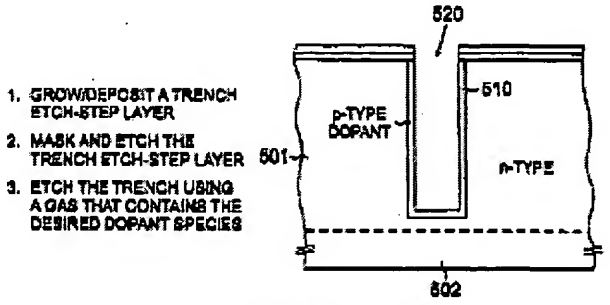


FIG. 4A

forming a plurality of spaced apart first doped regions **7, 8** of the first conductivity type (n-type) in the epitaxial layer; forming a plurality of first trenches **520** in the epitaxial layer, wherein each first trench **520** is between a pair of first doped regions **7, 8** (col. 4, lines 58-65 and FIG. 5);

doping at least portions of sidewall surfaces and lower surfaces of each second trench to form a plurality of doped gate regions **512**, wherein the plurality of doped gate regions extend into the body of compound semiconductor material **501** (col. 4, lines 50-65 and FIG. 4B);

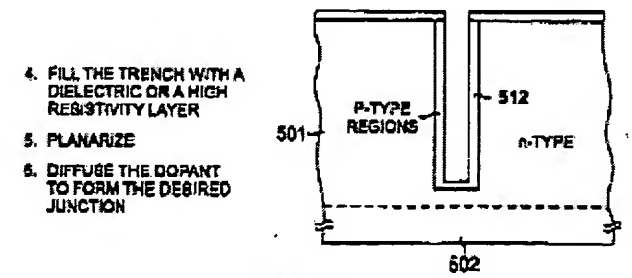
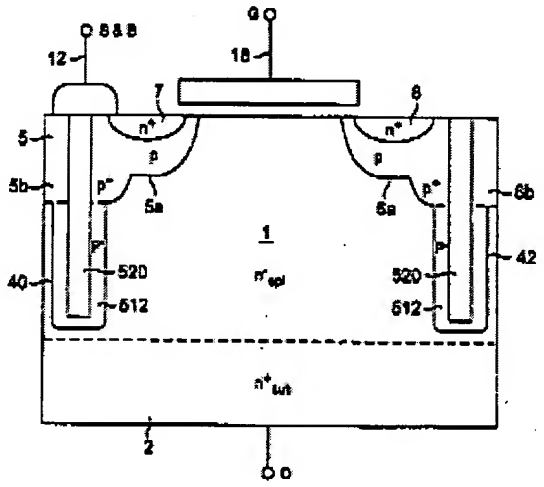


FIG. 4B

filling the plurality of second trenches and at least a portion of the first plurality of trenches with a passivation material (col. 4, lines 58-65 and FIG. 5);

coupling the plurality of spaced apart first doped regions **7, 8** with a first contact layer; coupling the plurality of doped gate regions **512** to a gate connecting region formed in the body of compound semiconductor mateial; and forming a drain contact **D** on a lower surface of the support wafer 2 (col. 5, lines 23-54 and FIG. 5);



THE DOPANT DISTRIBUTION OF A HIGH VOLTAGE VERTICAL DMOS TRANSISTOR WITH A RELATIVELY LOW ON-RESISTANCE

FIG. 5

Blanchard et al. '104 does not explicitly disclose forming a plurality of second trenches in the epitaxial layer, wherein one second trench is within one first trench.

Blanchard '058, however, discloses a method of making a semiconductor vertical FET device comprising the steps of: providing a body of semiconductor material comprising a first conductivity type (n-type), wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact; forming a first trench **31** in the body of semiconductor

material and extending from the upper surface, wherein the first trench has a first width (unlabeled), a first depth (unlabeled) from the upper surface, first sidewalls **41**, and a first bottom surface **42** (col. 3, line 60 to col. 5, line 3 and FIGS. 4a-b);

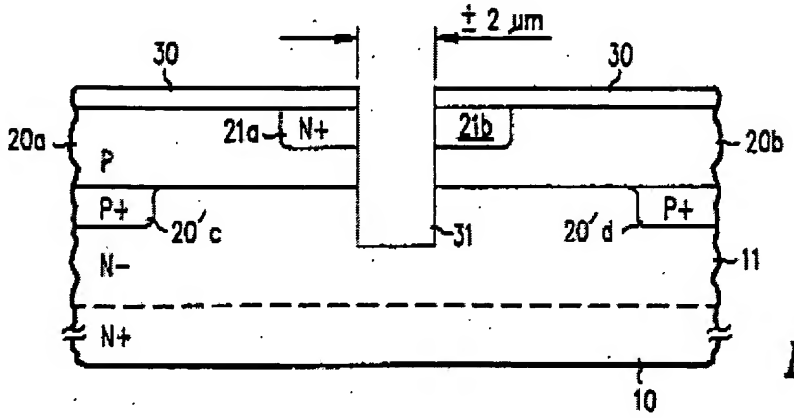


FIG. 4b

forming a second trench (unlabeled) within the first trench, wherein the second trench has a second width (unlabeled), a second depth (unlabeled) from the first surface, second sidewalls **43** and a second bottom surface **42a** (col. 5, lines 4-32 and FIG. 4g);

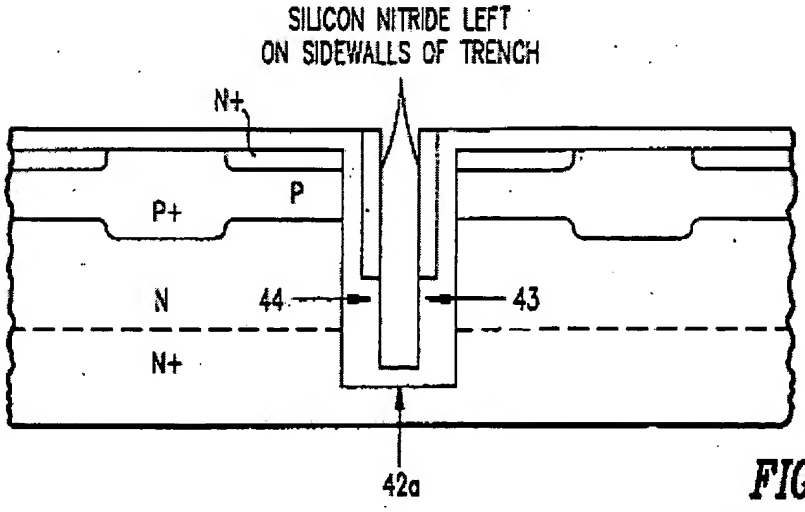


FIG. 4g

forming a first source region **21a** in the body of semiconductor material extending from the upper surface and spaced apart from the first trench (col. 5, line 33 to col. 6, line 37 and FIGS 3-10).

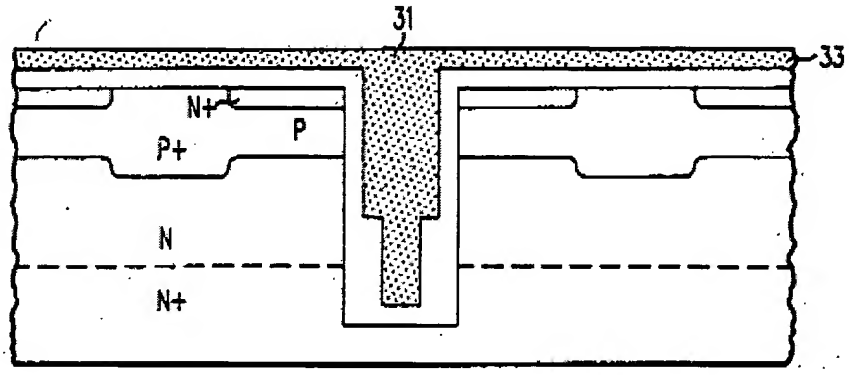


FIG. 4h

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Blanchard et al. '104 and Blanchard '058 to enable the process of forming a second trench within the first trench of Blanchard et al. '104 to be performed and furthermore to obtain a device which has a vertical gate and a planar surface (col. 2, lines 16-20, Blanchard '058).

In re claim 19, **Tews et al.** (U.S. Patent 6,335,247) provide evidence that the process of providing the body of compound semiconductor material includes providing a body of compound semiconductor material comprising one of GaAs (gallium arsenide) and InP is well-known to one of ordinary skill in the art at the time of the invention was made (col. 5, lines 12-33 and FIG. 3A).

In re claim 20, **Blanchard et al.** '104 disclose that the step of doping the sidewall surfaces and lower surfaces includes ion implanting a dopant of the second conductivity type dopant species (n-type) (col. 4, lines 50-65 and FIG. 4B).

Response to Applicant's Amendment and Arguments

Applicant contends that the Blanchard and Yanagisawa references fail to make the claims obvious for at least the following reasons. Specifically, both reference fail to show or suggest a source region spaced apart from the first trench by a portion of the body of semiconductor material.

In response to Applicant's contention that the Blanchard and Yanagisawa references fail to show or suggest a source region spaced apart from the first trench by a portion of the body of semiconductor material, Examiner respectfully submits that Applicant's argument is moot in view of the newly discovered reference to Blanchard et al. (U.S. Patent 6,750,104). As shown in (col. 4, lines 50-65 and FIG. 4B), Blanchard et al. disclose forming a first source region **7** in the body of semiconductor material **501** extending from the upper surface and spaced apart from the first trench **520** by a portion of the body of semiconductor material; introducing a dopant (Boron) of a second conductivity type (p-type) into at least a portion of the second sidewalls and the second bottom surface to form a doped gate region **512** wherein the doped gate region extends into the body of the semiconductor material (col. 4, lines 50-65 and FIG. 4B);

For this reason, Examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
July 24th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER